7-27-06

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Attorney 17419US01

In the Application of: MacInnis	**EXPRESS MAILING NO.: EV 726845922US**
U.S. Serial No.: 09/642,458	DATED: July 26, 2006
Filed: Aug. 18, 2000	
For: Video and Graphics System with an Integrated System Bridge Controller	
Examiner: Y Lee	
Group Art Unit: 2613	

APPEAL BRIEF

Mail Stop Appeal Brief – Patents
Commissioner for Patents
P.O. Box 1450
Alexandria VA 22313-1450

Sir:

This is an appeal from the Office Action made Final mailed December 12, 2005 in which claims 1-3, 5-39, 41, 49-51, 53, and 54 were rejected. A Notice of Appeal was filed with the United States Patent and Trademark Office on February 22, 2006. The deadline for filing this appeal brief is August 22, 2006, pursuant to Appellant's petition for a four-month extension filed concurrently herewith.

TABLE OF CONTENTS

I. REAL PARTY IN INTEREST

Broadcom Corporation, a corporation organized under the laws of the state of California and having a place of business at 16215 Alton Parkway, Irvine California 92618-3616, has acquired the entire right, title, and interest in and to the invention, the application, and any and all patents to be obtained therefore, as set forth in the Assignment filed with the present application and recorded on March 12, 2001 at Reel/Frame 011583/0685.

II. RELATED APPEALS AND INTERFERENCES

None.

III. STATUS OF THE CLAIMS

Claim 1 is rejected under 35 U.S.C. 102(e).
Claims 2 and 3 are rejected under 35 U.S.C. 103(a).
Claim 4 is cancelled without prejudice.
Claims 5 and 6 are rejected under 35 U.S.C. 102(e).
Claims 7 and 8 are rejected under 35 U.S.C. 103(a).
Claims 9-11 are rejected under 35 U.S.C. 102(e).
Claims 12-13 are rejected under 35 U.S.C. 103(a).
Claims 14-17 are rejected under 35 U.S.C. 102(e).
Claims 18-19 are rejected under 35 U.S.C. 103(a).
Claims 20-22 are rejected under 35 U.S.C. 102(e).
Claim 23 is rejected under 35 U.S.C. 103(a).
Claim 24 is rejected under 35 U.S.C. 102(e).
Claim 25 is rejected under 35 U.S.C. 103(a).
Claims 26-27 are rejected under 35 U.S.C. 102(e).
Claims 28-29 are rejected under 35 U.S.C. 103(a).
Claims 30-32 are rejected under 35 U.S.C. 102(e).
Claims 33-34 are rejected under 35 U.S.C. 103(a).

Claims 35-36 are rejected under 35 U.S.C. 102(e).

Claims 37-38 are rejected under 35 U.S.C. 103(a).

Claim 39 is rejected under 35 U.S.C. 102(e).

Claim 40 is cancelled without prejudice.

Claims 41 is rejected under 35 U.S.C. 102(e).

Claims 42-48 are cancelled without prejudice.

Claim 49 is rejected under 35 U.S.C. 103(a).

Claims 50-51 are rejected under 35 U.S.C. 102(e).

Claim 52 is cancelled without prejudice.

Claims 53 and 54 are rejected under 35 U.S.C. 102(e).

IV. STATUS OF AMENDMENTS

There are no amendments pending in the present application.

V. SUMMARY OF THE INVENTION

Certain embodiments of the present invention may comprise a system on single integrated circuit chip comprising an MPEG Transport processor, an MPEG video decoder, a display engine, and a system bridge controller. The MPEG Transport processor receives a plurality of MPEG Transport streams, at least one of the MPEG Transport streams including MPEG video data. The MPEG video decoder decodes the MPEG video data using an external memory to generate video for displaying. The display engine processes graphics to be blended with the video using the external memory. The system bridge controller has a north bridge function disposed between a CPU and a plurality of peripheral devices for coupling the CPU to the plurality of peripheral devices. The MPEG video decoder, the display engine and the system bridge controller are implemented on the single integrated circuit chip. The plurality of peripheral devices are situated externally to the single integrated circuit chip. The external memory has a unified memory architecture, such that the external memory is

concurrently used by the CPU through the system bridge controller as at least a part of its main memory, the display engine for processing the graphics, and the MPEG decoder for decoding the MPEG video data.

Certain embodiments are directed to a method of coupling a CPU to other devices and to process MPEG video data. The method comprises coupling the CPU to a plurality of peripheral devices via a system bridge controller having a north bridge function implemented on an integrated circuit chip, receiving a plurality of MPEG Transport streams using an MPEG Transport processor implemented on the integrated circuit chip, at least one of the MPEG Transport streams including the MPEG video data; and decoding the MPEG video data using an MPEG video decoder implemented on the integrated circuit chip to generate video for displaying, wherein the plurality of peripheral devices are situated externally to the integrated circuit chip.

Certain embodiments are directed to a system on a single integrated circuit chip comprising an MPEG Transport processor, an MPEG video decoder, and a system bridge controller. The MPEG Transport processor receives a plurality of MPEG Transport streams, at least one of the MPEG Transport streams including MPEG video data. The MPEG video decoder processes the MPEG video data to generate video for displaying. The system bridge controller has a north bridge function disposed between a CPU and a plurality of peripheral devices for coupling the CPU to at least one of the MPEG Transport processor and the MPEG video decoder, and to the plurality of peripheral devices. The MPEG Transport processor, the MPEG video decoder and the system bridge controller are implemented on the single integrated circuit chip. The plurality of peripheral devices are situated externally to the single integrated circuit chip.

Claim 1 is directed to a system on a single integrated circuit chip comprising: an MPEG Transport processor for receiving a plurality of MPEG Transport streams, at least one of the MPEG Transport streams including MPEG video data; an MPEG video decoder for decoding the MPEG video data using an external memory to generate video for displaying; a display engine for processing graphics to be blended with the video using the external memory; and a system

bridge controller having a north bridge function disposed between a CPU and a plurality of peripheral devices for coupling the CPU to the plurality of peripheral devices, wherein the MPEG video decoder, the display engine and the system bridge controller are implemented on the single integrated circuit chip, wherein the plurality of peripheral devices are situated externally to the single integrated circuit chip, and wherein the external memory has a unified memory architecture, such that the external memory is concurrently used by the CPU through the system bridge controller as at least a part of its main memory, the display engine for processing the graphics, and the MPEG decoder for decoding the MPEG video data.

Exemplary embodiments of claim 1 are described in the specification, for example, a system on a single integrated circuit (Figure 39, 1400), an MPEG Transport processor (1506) for receiving a plurality of MPEG Transport streams (1530), at least one of the MPEG Transport streams including MPEG video data; an MPEG video decoder (1504) for decoding the MPEG video data using an external memory (Figure 38, 1402) to generate video for displaying, a display engine (Figure 39, 1516) for processing graphics to be blended with the video using the external memory (Figure 38, 1504), and a system bridge controller (1508), having a north bridge function disposed between a CPU (Figure 38, 1406) and a plurality of peripheral devices (1422) for coupling the CPU to the plurality of peripheral devices, wherein the MPEG video decoder, (Figure 39, 1504) the display engine (1516) and the system bridge controller (1508) are implemented on the single integrated circuit chip (see Figure 39), wherein the plurality of peripheral devices are situated externally to the single integrated circuit chip (see Figure 38), and wherein the external memory has a unified memory architecture, such that the external memory is concurrently used by the CPU through the system bridge controller as at least a part of its main memory, the display engine for processing the graphics, and the MPEG decoder for decoding the MPEG video data (page 124, lines 5-11).

Claim 22 is directed to a method of coupling a CPU to other devices and to process MPEG video data. The method comprises coupling the CPU to a

plurality of peripheral devices via a system bridge controller having a north bridge function implemented on an integrated circuit chip, receiving a plurality of MPEG Transport streams using an MPEG Transport processor implemented on the integrated circuit chip, at least one of the MPEG Transport streams including the MPEG video data; and decoding the MPEG video data using an MPEG video decoder implemented on the integrated circuit chip to generate video for displaying, wherein the plurality of peripheral devices are situated externally to the integrated circuit chip.

Exemplary embodiments of claim 22 are described in the specification, for example, a method of coupling a CPU (Figure 38, 1406) to other devices (1422) and to process MPEG video data. The method comprises coupling the CPU (1422) to a plurality of peripheral devices (1422) via a system bridge controller (Figure 39, 1508) having a north bridge function implemented on an integrated circuit chip (1400), receiving a plurality of MPEG Transport streams using an MPEG Transport processor (1506) implemented on the integrated circuit chip (1400), at least one of the MPEG Transport streams including the MPEG video data; and decoding the MPEG video data using an MPEG video decoder (1504) implemented on the integrated circuit chip to generate video for displaying, wherein the plurality of peripheral devices are situated externally to the integrated circuit chip.

Claim 41 is directed to a system on a single integrated circuit chip comprising: an MPEG Transport processor for receiving a plurality of MPEG Transport streams, at least one of the MPEG Transport streams including MPEG video data; an MPEG video decoder for processing the MPEG video data to generate video for displaying; a system bridge controller having a north bridge function disposed between a CPU and a plurality of peripheral devices for coupling the CPU to at least one of the MPEG Transport processor and the MPEG video decoder, and to the plurality of peripheral devices, wherein the MPEG Transport processor, the MPEG video decoder and the system bridge controller are implemented on the single integrated circuit chip, and wherein the

plurality of peripheral devices are situated externally to the single integrated circuit chip.

Exemplary embodiments of claim 41 can be found in the specification, for example, a system on a single integrated circuit chip (Figure 39, 1400) comprising: an MPEG Transport processor (1506) for receiving a plurality of MPEG Transport streams (1530), at least one of the MPEG Transport streams including MPEG video data; an MPEG video decoder (1504) for processing the MPEG video data to generate video for displaying; a system bridge controller (1508) having a north bridge function disposed between a CPU (Figure 38, 1406) and a plurality of peripheral devices (1422) for coupling the CPU to at least one of the MPEG Transport processor and the MPEG video decoder, and to the plurality of peripheral devices, wherein the MPEG Transport processor, the MPEG video decoder and the system bridge controller are implemented on the single integrated circuit chip (see Figure 39), and wherein the plurality of peripheral devices are situated externally to the single integrated circuit chip (see Figure 38).

VI. ISSUES FOR REVIEW

Whether claims 1, 5, 6, 9-11, 14-17, 20-22, 24, 26, 27, 30-32, 35-36, 39, 41, 50-51, and 54 are unpatentable under 35 U.S.C. 102(e) as being anticipated from U.S. Patent 5,909,559 to So ("So").

Whether claims 2, 3, 7, 8, 12, 13, 18, 19, 23, 25, 28, 29, 33, 34, 37, 38 and 49 are unpatentable under 35 U.S.C. 103(a) as being obvious from the combination of So and Yee.

VII. ARGUMENT - CLAIM 1

Claims 1 stands rejected under 35 U.S.C. 102(e) as being anticipated by So.

Claim 1 is reproduced as follows:

1. A system on a single integrated circuit chip comprising:

an MPEG Transport processor for receiving a plurality of MPEG Transport streams, at least one of the MPEG Transport streams including MPEG video data;

an MPEG video decoder for decoding the MPEG video data using an external memory to generate video for displaying;

a display engine for processing graphics to be blended with the video using the external memory; and

a system bridge controller having a north bridge function disposed between a CPU and a plurality of peripheral devices for coupling the CPU to the plurality of peripheral devices,

wherein the MPEG video decoder, the display engine and the system bridge controller are implemented on the single integrated circuit chip,

wherein the plurality of peripheral devices are situated externally to the single integrated circuit chip, and

wherein the external memory has a unified memory architecture, such that the external memory is concurrently used by the CPU through the system bridge controller as at least a part of its main memory, the display engine for processing the graphics, and the MPEG decoder for decoding the MPEG video data.

To anticipate a claim, the reference must teach every element of the claim. "A claim is anticipated only if each and every element as set forth in the claimed is found, either expressly or inherently described, in a single prior art reference. *Verdegaal Bros. V. Union Oil Co. of California*, 814 F.2d 628, 631 (Fed. Cir. 1987)." MPEP 2131. Appellants respectfully submit that each and

every element as set forth in claims 1 and 41 are not found, either expressly or inherently described, in So.

A. The rejection to claim 1 should be reversed because So does not teach "an MPEG Transport processor for receiving a plurality of MPEG Transport streams, at least one of the MPEG Transport streams including MPEG video data."

Examiner has indicated that "since the So reference discusses using the single chip in set-top boxes which are used to receive cable broadcasts then So teaches MPE[G] transport streams are received by the set-top box which includes the single integrated chip that also decompresses MPEG. Refer to the following definition of a set-top box which may be found at [the "WhatIs?" web page]."[1] Examiner also makes reference to a Cisco web page ("Cisco").[2]

Examiner has not indicated that So expressly describes "an MPEG Transport Processor for receiving a plurality of MPEG Transport streams, at least one of the MPEG Transport streams including video data". Rather, Examiner has indicated that "So discusses using the single chip in set-top boxes" and that "In the third paragraph [of Whatis?] this discussion state the set-top box processes an MPEG transport stream."[3]

Appellant submits that even if Whatis? and Cisco taught a set top box that "processes an MPEG transport stream", it does not follow that the set top box in So includes "an MPEG Transport processor for receiving a plurality of MPEG Transport streams". Where the Whatis? reference indicates that "In the DTV realm, a typical digital set-top box contains one or more microprocessors for running the operating system, possibly Linux or Windows CE, and for parsing the MPEG transport stream" (Emphasis Added), it not only fails to indicate that set-top boxes by definition or inherently include "a transport processor for receiving a

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[1] Final Office Action ("F.O.A."), December 12, 2005 p. 2.

[2] F.O.A., p. 3.

[3] F.O.A., p. 2,3.

transport stream", but it also indicates that a set top box might not have "a transport processor for receiving a transport stream".

The fact that a certain result or characteristic may occur or be present in the prior art is not sufficient to establish the inherency of that result or characteristic. *In re Rijckaert*, 9 F.3d 1531, 1534, 28 USPQ2d 1955, 1957 (Fed. Cir. 1993) (reversed rejection because inherency was based on what would result due to optimization of conditions, not what was necessarily present in the prior art); *In re Oelrich*, 666 F.2d 578, 581-82, 212 USPQ 323, 326 (CCPA 1981). "To establish inherency, the extrinsic evidence 'must make clear that the missing descriptive matter is necessarily present in the thing described in the reference, and that it would be so recognized by persons of ordinary skill. Inherency, however, may not be established by probabilities or possibilities. The mere fact that a certain thing may result from a given set of circumstances is not sufficient.' " *In re Robertson*, 169 F.3d 743, 745, 49 USPQ2d 1949, 1950-51 (Fed. Cir. 1999) (citations omitted)".[4]

Thus the mere fact that So teaches a set top box taught does not mean that So teaches "an MPEG Transport processor for receiving a plurality of MPEG Transport streams, at least one of the MPEG Transport streams including MPEG video data." For at least the foregoing reason, the Board is respectfully requested to reverse to rejection to claim 1.

B. Even if So's teaching of a "Set Top Box" included an MPEG Transport Processor", So does not teach that "MPEG Transport Processor" would be included on the "single integrated circuit" that also comprises "the MPEG Video Decoder", "display engine", and "system bridge controller".

Examiner has indicated that the "since the So reference discusses using the single chip in set-top boxes which are used to receive cable broadcasts then So teaches MPEG transport streams are received by the set-top box which includes the single integrated chip that also decompresses MPEG."

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[4] MPEP 2112.

Appellants disagree with Examiner's characterization of the So reference as teaching "using the single chip in set-top boxes". Rather, So teaches, e.g., at Col. 133, Lines 58-65, "a north bridge/type block 610 has a first VSP core enhancing the north bridge PCI/MCU circuitry and that first VSP runs 3D geometry and multimedia extensions acceleration. A second VSP block 620 virtualizes 3D audio, graphics, slop/setup and MPEG audio/video compression/decompression. Blocks 610 and 620 are integrated together into a single integrated circuit chip...". So's teaching that "Blocks 610 and 620", neither of which include "a transport processor" "are integrated together", does not amount to a teaching of "using the single chip in set-top boxes". Moreover, So, Figure 6 shows several items that are not included the chip that integrates blocks 610 and 620. Accordingly, even if the "set-top box" in So included a "transport processor", So does not teach that the "transport processor" is included where "Blocks 610 and 620 are integrated together into a single integrated circuit chip."

Accordingly, for at least the foregoing reasons, Appellant respectfully requests that the Board reverse the rejection to claim 1.

VIII. CLAIMS 41, 2, 3,5-21, 49, 53, AND 54

Claims 41 stands rejected under 35 U.S.C. 102(e) as being anticipated by So.

Claim 41 is reproduced as follows:

A system on a single integrated circuit chip comprising:

an MPEG Transport processor for receiving a plurality of MPEG Transport streams, at least one of the MPEG Transport streams including MPEG video data;

an MPEG video decoder for processing the MPEG video data to generate video for displaying;

a system bridge controller having a north bridge function disposed between a CPU and a plurality of peripheral devices for coupling the CPU to at least one of the MPEG Transport processor and the MPEG video decoder, and to the plurality of peripheral devices, wherein the MPEG Transport processor, the MPEG video decoder and the system bridge controller are implemented on the single integrated circuit chip, and

wherein the plurality of peripheral devices are situated externally to the single integrated circuit chip.

To anticipate a claim, the reference must teach every element of the claim. "A claim is anticipated only if each and every element as set forth in the claimed is found, either expressly or inherently described, in a single prior art reference. *Verdegaal Bros. V. Union Oil Co. of California*, 814 F.2d 628, 631 (Fed. Cir. 1987)." MPEP 2131. Appellants respectfully submit that each and every element as set forth in claims 1 and 41 are not found, either expressly or inherently described, in So.

A. The rejection to claim 41 should be reversed because So does not teach "an MPEG Transport processor for receiving a plurality of MPEG Transport streams, at least one of the MPEG Transport streams including MPEG video data."

Examiner has indicated that "since the So reference discusses using the single chip in set-top boxes which are used to receive cable broadcasts then So teaches MPE[G] transport streams are received by the set-top box which includes the single integrated chip that also decompresses MPEG. Refer to the following definition of a set-top box which may be found at [the "WhatIs?" web page]."[5] Examiner also makes reference to a Cisco web page ("Cisco").[6]

Examiner has not indicated that So expressly describes "an MPEG Transport Processor for receiving a plurality of MPEG Transport streams, at least one of the MPEG Transport streams including video data". Rather, Examiner has indicated that "So discusses using the single chip in set-top boxes" and that "In the third paragraph [of Whatis?] this discussion state the set-top box processes an MPEG transport stream."[7]

Appellant submits that even if Whatis? and Cisco taught a set top box that "processes an MPEG transport stream", it does not follow that the set top box in So includes "an MPEG Transport processor for receiving a plurality of MPEG Transport streams". Where the Whatis? reference indicates that "In the DTV realm, a typical digital set-top box contains one or more microprocessors for running the operating system, possibly Linux or Windows CE, and for parsing the MPEG transport stream" (Emphasis Added), it not only fails to indicate that set-top boxes by definition or inherently include "a transport processor for receiving a transport stream", but it also indicates that a set top box might not have "a transport processor for receiving a transport stream".

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[5] Final Office Action ("F.O.A."), December 12, 2005 p. 2.

[6] F.O.A., p. 3.

[7] F.O.A., p. 2,3.

The fact that a certain result or characteristic may occur or be present in the prior art is not sufficient to establish the inherency of that result or characteristic. *In re Rijckaert*, 9 F.3d 1531, 1534, 28 USPQ2d 1955, 1957 (Fed. Cir. 1993) (reversed rejection because inherency was based on what would result due to optimization of conditions, not what was necessarily present in the prior art); *In re Oelrich*, 666 F.2d 578, 581-82, 212 USPQ 323, 326 (CCPA 1981). "To establish inherency, the extrinsic evidence 'must make clear that the missing descriptive matter is necessarily present in the thing described in the reference, and that it would be so recognized by persons of ordinary skill. Inherency, however, may not be established by probabilities or possibilities. The mere fact that a certain thing may result from a given set of circumstances is not sufficient.' " *In re Robertson*, 169 F.3d 743, 745, 49 USPQ2d 1949, 1950-51 (Fed. Cir. 1999) (citations omitted)".[8]

Thus the mere fact that So teaches a set top box taught does not mean that So teaches "an MPEG Transport processor for receiving a plurality of MPEG Transport streams, at least one of the MPEG Transport streams including MPEG video data." For at least the foregoing reason, the Board is respectfully requested to reverse to rejection to claim 41 and dependent claims 2, 3,5-21, 49, 53, and 54.

B. Even if So's teaching of a "Set Top Box" included an MPEG Transport Processor", So does not teach that "MPEG Transport Processor" would be included on the "single integrated circuit" that also comprises "the MPEG Video Decoder", "display engine", and "system bridge controller".

Examiner has indicated that the "since the So reference discusses using the single chip in set-top boxes which are used to receive cable broadcasts then So teaches MPEG transport streams are received by the set-top box which includes the single integrated chip that also decompresses MPEG."

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[8] MPEP 2112.

Appellants disagree with Examiner's characterization of the So reference as teaching "using the single chip in set-top boxes". Rather, So teaches, e.g., at Col. 133, Lines 58-65, "a north bridge/type block 610 has a first VSP core enhancing the north bridge PCI/MCU circuitry and that first VSP runs 3D geometry and multimedia extensions acceleration. A second VSP block 620 virtualizes 3D audio, graphics, slop/setup and MPEG audio/video compression/decompression. Blocks 610 and 620 are integrated together into a single integrated circuit chip...". So's teaching that "Blocks 610 and 620", neither of which include "a transport processor" "are integrated together", does not amount to a teaching of "using the single chip in set-top boxes". Moreover, So, Figure 6 shows several items that are not included the chip that integrates blocks 610 and 620. Accordingly, even if the "set-top box" in So included a "transport processor", So does not teach that the "transport processor" is included where "Blocks 610 and 620 are integrated together into a single integrated circuit chip."

Accordingly, for at least the foregoing reasons, Appellant respectfully requests that the Board reverse the rejection to claim 41 and dependent claims 2, 3, 5-21, 49, 53, and 54.

IX. CLAIM 20.

Claim 20 stands rejected under 35 U.S.C. 102(e) as anticipated by So.

Claim 20 is reproduced as follows:

The system of claim 41 wherein the video includes at least one HDTV.

The arguments made in Section VIII are incorporated herein.

Furthermore, Appellant additionally requests that the board reverse the rejection to claim 20 because So does not teach "wherein the video includes at least one HDTV".

Examiner has indicated that "HDTV means high definition TV which is inferred by reference[d] to television at column 129, line 31. So, Column 129,

Line 31 merely discusses a "television set". Examiner argues that "the term television includes many television standards including HDTV".[9]

To anticipate a claim, the reference must teach every element of the claim. "A claim is anticipated only if each and every element as set forth in the claimed is found, either expressly or inherently described, in a single prior art reference. *Verdegaal Bros. V. Union Oil Co. of California*, 814 F.2d 628, 631 (Fed. Cir. 1987)." MPEP 2131. So does not expressly describe HDTV. Moreover, Examiner's argument that the "term television includes many television standards including HDTV" establishes that it is not inherently described.

It would appear that Examiner is attempting the logical fallacy of anticipating a species by the disclosure of its genus.

For at least the foregoing reasons, Appellant respectfully request that the Board reverse the rejection to claim 20.

X. CLAIM 22-39

Claim 22 stands rejected under 35 U.S.C. 102(e) as being anticipated by So.

Claim 22 is reproduced as follows:

A method of coupling a CPU to other devices and to process MPEG video data, the method comprising:

coupling the CPU to a plurality of peripheral devices via a system bridge controller having a north bridge function implemented on an integrated circuit chip,

receiving a plurality of MPEG Transport streams using an MPEG Transport processor implemented on the integrated circuit chip, at least one of the MPEG Transport streams including the MPEG video data; and

decoding the MPEG video data using an MPEG video decoder implemented on the integrated circuit chip to generate video for displaying,

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[9] F.O.A., p. 4 (See Remarks regarding claim "30", which appears to be a typographical error where claim 20 is meant).

wherein the plurality of peripheral devices are situated externally to the integrated circuit chip.

To anticipate a claim, the reference must teach every element of the claim. "A claim is anticipated only if each and every element as set forth in the claimed is found, either expressly or inherently described, in a single prior art reference. *Verdegaal Bros. V. Union Oil Co. of California*, 814 F.2d 628, 631 (Fed. Cir. 1987)." MPEP 2131. Appellants respectfully submit that each and every element as set forth in claims 1 and 41 are not found, either expressly or inherently described, in So.

A. The rejection to claim 22 should be reversed because So does not teach "receiving a plurality of MPEG Transport streams using an MPEG Transport processor implemented on the integrated circuit chip, at least one of the MPEG Transport streams including the MPEG video data"

Examiner has indicated that "since the So reference discusses using the single chip in set-top boxes which are used to receive cable broadcasts then So teaches MPE[G] transport streams are received by the set-top box which includes the single integrated chip that also decompresses MPEG. Refer to the following definition of a set-top box which may be found at [the "WhatIs?" web page]."[10] Examiner also makes reference to a Cisco web page ("Cisco").[11]

Examiner has not indicated that So expressly describes "an MPEG Transport Processor for receiving a plurality of MPEG Transport streams, at least one of the MPEG Transport streams including video data". Rather, Examiner has indicated that "So discusses using the single chip in set-top boxes" and that "In

[10] Final Office Action ("F.O.A."), December 12, 2005 p. 2.

[11] F.O.A., p. 3.

the third paragraph [of Whatis?] this discussion state the set-top box processes an MPEG transport stream."[12]

Appellant submits that even if Whatis? and Cisco taught a set top box that "processes an MPEG transport stream", it does not follow that the set top box in So includes "an MPEG Transport processor for receiving a plurality of MPEG Transport streams". Where the Whatis? reference indicates that "In the DTV realm, a typical digital set-top box contains one or more microprocessors for running the operating system, possibly Linux or Windows CE, and for parsing the MPEG transport stream" (Emphasis Added), it not only fails to indicate that set-top boxes by definition or inherently include "a transport processor for receiving a transport stream", but it also indicates that a set top box might not have "a transport processor for receiving a transport stream".

The fact that a certain result or characteristic may occur or be present in the prior art is not sufficient to establish the inherency of that result or characteristic. *In re Rijckaert*, 9 F.3d 1531, 1534, 28 USPQ2d 1955, 1957 (Fed. Cir. 1993) (reversed rejection because inherency was based on what would result due to optimization of conditions, not what was necessarily present in the prior art); *In re Oelrich*, 666 F.2d 578, 581-82, 212 USPQ 323, 326 (CCPA 1981). "To establish inherency, the extrinsic evidence 'must make clear that the missing descriptive matter is necessarily present in the thing described in the reference, and that it would be so recognized by persons of ordinary skill. Inherency, however, may not be established by probabilities or possibilities. The mere fact that a certain thing may result from a given set of circumstances is not sufficient.' " *In re Robertson*, 169 F.3d 743, 745, 49 USPQ2d 1949, 1950-51 (Fed. Cir. 1999) (citations omitted)".[13]

Thus the mere fact that So teaches a set top box taught does not mean that So teaches "an MPEG Transport processor for receiving a plurality of MPEG Transport streams, at least one of the MPEG Transport streams including MPEG

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[12] F.O.A., p. 2,3.

[13] MPEP 2112.

video data." For at least the foregoing reason, the Board is respectfully requested to reverse to rejection to claim 22 and dependent claims 23-39.

B. Even if So's teaching of a "Set Top Box" included an MPEG Transport Processor", So does not teach that "MPEG Transport Processor" would be included on the "single integrated circuit" that also comprises "the MPEG Video Decoder", "display engine", and "system bridge controller".

Examiner has indicated that the "since the So reference discusses using the single chip in set-top boxes which are used to receive cable broadcasts then So teaches MPEG transport streams are received by the set-top box which includes the single integrated chip that also decompresses MPEG."

Appellants disagree with Examiner's characterization of the So reference as teaching "using the single chip in set-top boxes". Rather, So teaches, e.g., at Col. 133, Lines 58-65, "a north bridge/type block 610 has a first VSP core enhancing the north bridge PCI/MCU circuitry and that first VSP runs 3D geometry and multimedia extensions acceleration. A second VSP block 620 virtualizes 3D audio, graphics, slop/setup and MPEG audio/video compression/decompression. Blocks 610 and 620 are integrated together into a single integrated circuit chip...". So's teaching that "Blocks 610 and 620", neither of which include "a transport processor" "are integrated together", does not amount to a teaching of "using the single chip in set-top boxes". Moreover, So, Figure 6 shows several items that are not included the chip that integrates blocks 610 and 620. Accordingly, even if the "set-top box" in So included a "transport processor", So does not teach that the "transport processor" is included where "Blocks 610 and 620 are integrated together into a single integrated circuit chip."

Accordingly, for at least the foregoing reasons, Appellant respectfully requests that the Board reverse the rejection to claim 41 and dependent claims 23-39.

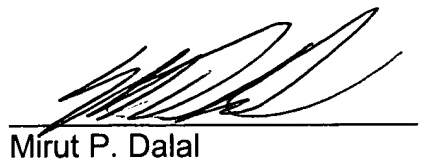
XI. CONCLUSION

For the foregoing reasons, all of the pending claims are distinguishable over the prior art of record. Reversal of the Examiner's rejection and issuance of a patent on the application are therefore requested.

The Commissioner is hereby authorized to charge $500 for the Appeal Brief fee and any additional fees or credit any overpayment to the deposit account of McAndrews, Held & Malloy, Account No. 13-0017.

Dated: July 26, 2006

Respectfully submitted,



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CLAIMS APPENDIX

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1. A system on a single integrated circuit chip comprising:

an MPEG Transport processor for receiving a plurality of MPEG Transport streams, at least one of the MPEG Transport streams including MPEG video data;

an MPEG video decoder for decoding the MPEG video data using an external memory to generate video for displaying;

a display engine for processing graphics to be blended with the video using the external memory; and

a system bridge controller having a north bridge function disposed between a CPU and a plurality of peripheral devices for coupling the CPU to the plurality of peripheral devices,

wherein the MPEG video decoder, the display engine and the system bridge controller are implemented on the single integrated circuit chip,

wherein the plurality of peripheral devices are situated externally to the single integrated circuit chip, and

wherein the external memory has a unified memory architecture, such that the external memory is concurrently used by the CPU through the system bridge controller as at least a part of its main memory, the display engine for processing the graphics, and the MPEG decoder for decoding the MPEG video data.

2. The system of claim 41 wherein the system bridge controller is capable of performing format conversion between big-endian data and little-endian data, between the CPU and one or more of the plurality of peripheral devices.

3. The system of claim 2 further comprising other components for processing video and graphics on the single integrated circuit chip, and wherein the system bridge controller is capable of performing format conversion between big-endian data and little-endian data, between the CPU and at least one of the

MPEG video decoder and the other components for processing video and graphics.

4. (Canceled)

5. The system of claim 41 wherein the plurality of peripheral devices include one or more PCI devices, and wherein the system bridge controller includes a PCI bridge for coupling the CPU to the one or more PCI devices.

6. The system of claim 5 wherein the PCI bridge is capable of performing a DMA function between the one or more PCI devices and an external memory.

7. The system of claim 5 wherein the PCI bridge is capable of performing format conversion between big-endian data used in the CPU and little-endian data used in the one or more PCI devices.

8. The system of claim 5 wherein the PCI bridge is capable of performing format conversion between little-endian data used in the CPU and big-endian data used in the one or more PCI devices.

9. The system of claim 41 wherein the plurality of peripheral devices include one or more I/O devices, and wherein the system bridge controller includes an I/O bus bridge for coupling the CPU to the one or more I/O devices.

10. The system of claim 9 wherein the I/O bus bridge is capable of performing a DMA function between the CPU and the one or more I/O devices.

11. The system of claim 9 wherein the one or more I/O devices include a device selected from a group consisting of ROM, RAM, flash memory and 68000-compatible peripheral devices.

12. The system of claim 9 wherein the I/O bus bridge is capable of performing format conversion between big-endian data used in the CPU and little-endian data used in the one or more I/O devices.

13. The system of claim 9 wherein the I/O bus bridge is capable of performing format conversion between little-endian data used in the CPU and big-endian data used in the one or more I/O devices.

14. The system of claim 41 wherein the system bridge controller includes a CPU interface block for coupling the CPU to the MPEG video decoder.

15. The system of claim 14 wherein the CPU interface block is coupled with the CPU selected from a group consisting of a MIPS processor, an SH3 processor and an SH4 processor.

16. The system of claim 14 wherein the CPU interface block is capable of performing burst accesses of the CPU in both read and write directions.

17. The system of claim 14 wherein the CPU interface block includes one or more buffers used to resolve a speed difference between the CPU and external SDRAM devices.

18. The system of claim 14 wherein the CPU interface block is capable of performing format conversion between big-endian data used in the CPU and little-endian data used in the MPEG video decoder.

19. The system of claim 14 wherein the CPU interface block is capable of performing format conversion between little-endian data used in the CPU and big-endian data used in the MPEG video decoder.

20. The system of claim 41 wherein the video includes at least one HDTV video.

21. The system of claim 41 wherein the video includes at least one SDTV video.

22. A method of coupling a CPU to other devices and to process MPEG video data, the method comprising:

coupling the CPU to a plurality of peripheral devices via a system bridge controller having a north bridge function implemented on an integrated circuit chip,

receiving a plurality of MPEG Transport streams using an MPEG Transport processor implemented on the integrated circuit chip, at least one of the MPEG Transport streams including the MPEG video data; and

decoding the MPEG video data using an MPEG video decoder implemented on the integrated circuit chip to generate video for displaying,

wherein the plurality of peripheral devices are situated externally to the integrated circuit chip.

23. The method of claim 22 wherein coupling the CPU to a plurality of peripheral devices comprises performing format conversion between big-endian data and little-endian data, between the CPU and one or more of the plurality of peripheral devices.

24. The method of claim 22 wherein the integrated circuit chip contains one or more internal components, and the method further comprises coupling the CPU to at least one of the one or more internal components via the system bridge controller.

25. The method of claim 24 wherein coupling the CPU to at least one of the one or more internal components comprises performing format conversion

between big-endian data and little-endian data, between the CPU and at least one of the one or more internal components.

26. The method of claim 22 wherein coupling the CPU to a plurality of peripheral devices comprises the step of coupling the CPU to one or more PCI devices.

27. The method of claim 26 further comprising performing a DMA function between the one or more PCI devices and an external memory.

28. The method of claim 26 wherein coupling the CPU to one or more PCI devices comprises performing format conversion between big-endian data used in the CPU and little-endian data used in the one or more PCI devices.

29. The method of claim 26 wherein coupling the CPU to one more PCI devices comprises performing format conversion between little-endian data used in the CPU and big-endian data used in the one or more PCI devices.

30. The method of claim 22 wherein coupling the CPU to a plurality of peripheral devices comprises coupling the CPU to one or more I/O devices, the I/O devices being coupled to the integrated circuit chip via a bus different from a PCI bus.

31. The method of claim 30 wherein coupling the CPU to one or more I/O devices comprises performing a DMA function between the CPU and the one or more I/O devices.

32. The method of claim 30 wherein the one or more I/O devices include one or more devices selected from a group consisting of ROM, RAM, flash memory and 68000-compatible peripheral devices.

33. The method of claim 30 wherein coupling the CPU to one or more I/O devices comprises performing format conversion between big-endian data used in the CPU and little-endian data used in the one or more I/O devices.

34. The method of claim 30 wherein coupling the CPU to one or more I/O devices comprises performing format conversion between little-endian data used in the CPU and big-endian data used in the one or more I/O devices.

35. The method of claim 24 wherein coupling the CPU to at least one of the one or more internal components comprises performing burst accesses of the CPU in both read and write directions.

36. The method of claim 24 wherein coupling the CPU to at least one of the one or more internal components comprises resolving a speed difference between the CPU and external SDRAM devices.

37. The method of claim 24 wherein coupling the CPU to at least one of the one or more internal components comprises performing format conversion between big-endian data used in the CPU and little-endian data used in the MPEG video decoder.

38. The method of claim 24 wherein coupling the CPU to at least one of the one or more internal components comprises performing format conversion between little-endian data used in the CPU and big-endian data used in the MPEG video decoder.

39. The method of claim 22 wherein the video generated by decoding the MPEG video data includes at least one HDTV video.

40. (Canceled)

41. A system on a single integrated circuit chip comprising:

an MPEG Transport processor for receiving a plurality of MPEG Transport streams, at least one of the MPEG Transport streams including MPEG video data;

an MPEG video decoder for processing the MPEG video data to generate video for displaying;

a system bridge controller having a north bridge function disposed between a CPU and a plurality of peripheral devices for coupling the CPU to at least one of the MPEG Transport processor and the MPEG video decoder, and to the plurality of peripheral devices, wherein the MPEG Transport processor, the MPEG video decoder and the system bridge controller are implemented on the single integrated circuit chip, and

wherein the plurality of peripheral devices are situated externally to the single integrated circuit chip.

42-48. (Canceled)

49. The system of claim 41, wherein the system bridge controller is capable of performing format conversion between big-endian data and little-endian data, between the CPU and at least one of the MPEG Transport processor and the MPEG video decoder, and one or more of the plurality of peripheral devices.

50. The system of claim 9, wherein the CPU has a first data width that is a multiple of a second data width of at least one of the one or more I/O devices, and wherein the I/O bus bridge automatically converts a data access with the first data width by the CPU into multiple data accesses with the second data width to support said at least one of the one or more I/O devices having the second data width.

51. The method of claim 30, wherein the CPU has a first data width that is a multiple of a second data width of at least one of the one or more I/O

devices, and wherein coupling the CPU to one or more I/O devices comprises automatically converting a data access with the first data width by the CPU into multiple data accesses with the second data width to support said at least one of the one or more I/O devices having the second data width.

52. (Cancelled).

53. The system of claim 41, further comprising a video compositor implemented on the single integrated circuit chip, wherein the video compositor blends the video generated by the MPEG video decoder with graphics.

54. The system of claim 53, further comprising a graphics blender implemented on the single integrated circuit chip, wherein the graphics blender blends two or more graphics windows to generate the graphics provided to the video compositor.

EVIDENCE APPENDIX

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RELATED PROCEEDINGS APPENDIX

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